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UNITED STATES PATENT APPLICATION

of

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for an

COMMUTATION AND VELOCITY CONTROL SYSTEM FOR A BRUSHLESS DC MOTOR

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PRIORITY DATA

This application claims priority from a provisional application filed December 30, 2000 designated serial number 60/259,354 entitled *"Commutation and Velocity Control System For Brushless DC Motor"*. This application is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to DC brushless motors, and in particular to a commutation and velocity control system for a brushless DC motor.

Brushless DC motors are in widespread use. A brushless DC motor employs a permanently magnetized rotor and electronic commutation to switch current to appropriate stator windings to cause the rotor to rotate to follow switched magnetic poles in the stator windings. Brushless DC motors may be commutated by signals generated from the rotational velocity and position of the rotor to cause the appropriate stator winding to be switched to sustain rotation. Furthermore, brushless DC motors may be commutated by an external frequency source to cause the rotor to rotate at a rotational velocity synchronous with the external signal source. Mechanisms for detecting the rotational velocity and position of the rotor include resolver windings, Hall effect devices, optical position sensors, etc.

Brushless DC motors often achieve brushless commutation by the use of the resolver that is rotationally coupled to an armature shaft and a pair of resolver windings, respectively

producing output signals sineθ and cosineθ, where θ is the angular position of the shaft, which are used to control the windings for driving the armature. From these position signals, velocity must be derived in order to control the commutation.

There is a need for a simplified commutation and velocity control system for a brushless DC motor.

SUMMARY OF THE INVENTION

Briefly, according to an aspect of the present invention, a commutation and velocity control system of a brushless DC motor receives a velocity command signal and provides command signals to drive the brushless DC motor. The system includes a summer that receives the velocity command signal and a velocity feedback signal and provides a velocity error signal indicative of the difference. A velocity loop compensator receives the velocity error signal and provides a compensated velocity error signal. A magnitude sensing circuit senses the magnitude of the compensated velocity error signal and provides a velocity magnitude signal indicative thereof. A polarity sensing circuit senses the polarity of the compensated velocity error signal and provides a velocity polarity signal indicative thereof. The system also includes an integrated circuit having: (i) a velocity calculation circuit that receives a first sampled digitized signal indicative of resolver position at a first time and a second sampled digitized signal indicative of resolver position at a second time, and determines velocity based upon the difference between the first and second sampled digitized signals and provides a sensed digitized velocity signal indicative thereof; (ii) a commutation logic circuit that receives the first sampled digitized signal, the velocity magnitude signal and the velocity

polarity signal, and provides the command signal; and (iii) a counter that receives a signal indicative of the sensed digitized velocity signal and provides a pulse width modulated output signal indicative thereof. A filter receives the pulse width modulated output signal and generates the velocity feedback signal.

The present invention provides a simplified commutation and velocity control system for a brushless DC motor.

These and other objects, features and advantages of the present invention will become apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustration of a commutation and velocity control system for a brushless DC motor;

FIG. 2 is a block diagram illustration of the FPGA;

FIGs. 3-5 illustrates commutation logic tables resident in the FPGA of FIG. 2:

FIG. 6 is a simplified illustration of a bridge driver circuit; and

FIG. 7 is a block diagram illustration of the resolver folder over logic.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a block diagram illustration of a commutation and velocity control system 10 for a brushless DC motor 12. The system 10 receives a velocity command signal on a line 14, which for example may be provided by a control loop (not shown) that operates closed loop on

the position of an actuator 16 driven by the brushless DC motor 12. The velocity command signal is input to a summer 18 that computes the difference between the commanded velocity and actual velocity, which is provided by a velocity feedback signal on a line 20. The summer 18 provides an error signal on a line 22 indicative of the error between commanded and actual velocity. This error signal is input to a velocity loop compensator 24 that provides an analog velocity error signal (e.g., a voltage signal) on a line 26 to a comparator 28.

The comparator 28 also receives a signal on a line 30 from a digital-to-analog converter (DAC) 32. The output of the DAC 32 on the line 30 is a triangular waveform that allows the comparator 28 to provide a pulse-width-modulated (PWM) output signal on a line 34, whose pulse width is indicative of the magnitude of the velocity error signal on the line 26.

The PWM output signal on the line 34 is input to an application specific integrated circuit, such as for example a field programmable gate array (FPGA) 36. Significantly, the FPGA 36 provides command signals on lines 38 to control the brushless DC motor 12, and also provides a signed brushless DC motor rotor velocity signal on a line 40 for the analog velocity loop. The command signals on the lines 38 are output to a H-bridge driver circuit 42, which preferably includes a plurality of FETs arranged to drive the motor 12.

Since the PWM signal on the line 34 contains only information indicative of the magnitude of the velocity error, the system 10 also includes a comparator 44 that receives the velocity error signal on the line 26 to determine the direction/polarity of the error. That is, if the velocity error signal on the line 26 is positive, then the comparator 44 provides a Boolean signal (DIR) on a line 46 that is logical one. Otherwise, if the velocity error signal on the line 26 is negative, the comparator 44 provides a Boolean signal on the line 46 that is logical zero.

Therefore, the signals on the lines 34, 46 (PWM and DIR, respectively) together provide magnitude and polarity information indicative of the velocity error on the line 26.

To provide feedback information, the system 10 also includes a motor shaft position resolver 50. The resolver 50 provides a sine signal on a line 52 and a cosine signal on a line 54 to a resolver signal processing interface 56, which is configured as an RC bridge circuit. The sine and cosine signals from the resolver signal processing interface 56 are separated by $(2*\theta)-90^{\circ}$, where θ is in resolver degrees. If the sine and cosine signals on the lines 52, 54 respectively, indicate that θ is equal to 90°, the output of the RC bridge circuit 56 is $(2*90^{\circ})-90^{\circ}$, which is 90° electrical. The brushless DC motor 12 preferably has four pole pairs and the resolver has two pole pairs to accommodate a direct $(2*\theta)$ to electrical degrees. In this embodiment, resolver receives an excitation signal on a line 57, which is a 23.4375 KHz sine wave whose frequency is counted down in the FPGA 36 by 1024 from the 24 MHz clock. In this case the following equivalents apply:

One electrical cycle: 360 deg electrical	= 90 degrees mechanical	=180 deg res.
One resolver cycle: 360 deg. res.	= 180 deg mechanical	
One commutation step of six steps	= 60 deg electrical	= 30 degree res.

The RC bridge circuit 56 provides start and stop signals on lines 58, 60 to the FPGA 36. These signals control a counter located within FPGA that provides an indication of $(2*\theta)$, that is resolver position.

FIG. 2 is a block diagram illustration of the FPGA 36. The FPGA receives a clock pulse (e.g., 24 MHz) on a line 70. The clock signal is input to a counter(s) 72 that generates slower clock signals (e.g., 4 MHz and 23.4375 KHz) from the clock input. The FPGA also

includes an up/down counter 74 (e.g., a seven bit counter) that cycles between a one hundred (100) ascending and descending count (i.e., it steps from 0 counts to 100 counts in steps of one, and then from 100 to 0 in steps of one count, and then repeats). The up/down counter 74 provides a count signal on a line 76 to the DAC 32 (FIG. 1), which generates the triangle waveform provided on the line 30. For example, a 4 Mhz clock signal on a line 78 may be used to drive the up/down counter 74, such that a full cycle of two hundred steps results in the DAC 32 providing a triangle waveform having a frequency of 20 KHz.

The FPGA 36 receives the start and stop signals on the lines 58, 60, which are used to control a counter 80. This counter 80 (e.g., a ten bit counter) operates at a 23.4375 KHz rate (a 42.67 μsec.period) preferably on the negative edge zero crossing. Selection of the resolver pole count at one-half times the motor pole count and use of the RC bridge for pre-processing, the start signal on the line 58 is separated from the stop signal on the line 60 by $(2*\theta)$ degrees resolver (e.g., a four pole motor and a two pole resolver). The value $(2*\theta)$ is a direct measurement of the electrical angle, where the following relationships apply:

1. $(2*\theta)$ full scale = 360° degrees electrical = 180 degrees resolver;
2. the resolver excitation period is equal to 42.667 μsec.;
3. the counter is 10 bits (i.e., 1024 states);
4. the clock is 24 MHz; and
5. the resolver excitation is 23.4375 KHz derived from the 24 MHz clock.

Therefore, based upon these relationships (i.e., this embodiment), the commutation granularity is equal to $360^\circ/1024 = 0.3515625^\circ$ electrical/count. In addition for six step commutation (i.e., 60° electrical/step), in this embodiment the relationship between counts/step is [(60° electrical/step)/(0.3515625° electrical/count)], which is equal to 170.6667 counts/step. As a

result, as the resolver 50 (FIG. 1) rotates with the motor shaft, the angle and the value from the counter 80 change proportionally. Commutation state changes occur as the ten bit count value progresses past defined thresholds stored in the FPGA 36 in commutation logic tables 82. The commutation logic tables provide the output signals on the lines 38 that control the motor drive circuit 42 (FIG. 1) by providing the phase switching information (commutation) for the three phase brushless DC motor. By switching in the proper sequence, the motor 12 (FIG. 1) is provided energy to cause rotation of the permanent magnet rotor in either direction. Variation of the energy is by pulse width modulation of the commutation pulse.

The commutation logic tables 82 receive the signal indicative of velocity error polarity (i.e., DIR) on the line 46 and the signal on the line 34 indicative of the magnitude of the velocity error (i.e., PWM). The commutation logic tables 82 also receive a signal on a line 86 indicative of the resolver angle. This signal is provided by a latch 88 that receives a count signal on a line 90 from the counter circuit 80.

The commutation logic tables 82 determine the state of the motor driver circuit based upon the velocity error (i.e., the signal on the lines 46 and 34) and the resolver angle (i.e., the signals on the lines 86). FIG. 3 illustrates a commutation logic table for the case DIR=1 and PWM=1. FIG. 4 illustrates a commutation logic table for the case DIR=0 and PWM=1. FIG. 5 illustrates the commutation logic table for the case: (i) PWM=0 and DIR=0 and (ii) PWM=0 and DIR=1. FIG. 6 is a simplified block diagram illustration of the bridge driver circuit 42. The bridge driver circuit 42 includes a plurality of current switches (e.g., FETs) Q1-Q6 101-106 that drive the three phase brushless DC motor 12.

Referring now to FIGs. 3 and 6, if DIR=1, PWM=1 and the signal on the line 86 is

equal to 511 counts, then the current switches Q1-Q6 101-106 are positioned as set forth in column 108. Similarly, if the signal on the line 86 indicative of resolver angle is equal to 700 counts, then the current switches Q1-Q6 101-106 are positioned as set forth in column 110. FET off to FET on dead time may be required to avoid "H" bridge common leg high side switch (HSS) and low side switch (LSS) coincident "on" times. Dead Time avoids common "H" leg coincident FET switch "on" states. For example, the dead time may be 1.5 μsec to accommodate the rise and fall times of the FET drivers when reversing directions and when normal commutation for PWM=1 transitions to PWM=0.

Referring again to FIG. 2, to provide the feedback signal on the line 40 indicative of velocity, the FPGA also includes velocity calculation circuitry 120 that computes the velocity using two sampled position signals divided by time. Specifically, counter 122 (e.g., a divide by sixteen counter) receives the start signal on the line 58 and every sixteen start pulses, the counter 120 clocks a latch 124 to sample the count value on the line 90. As a result, the latch 124 is clocked at one-sixteenth the rate of the latch 88. In this embodiment the velocity calculations are updated every sixteenth position update. A summer 126 receives the count signal on the line 86 and a count signal on a line 128 from the latch 124, and provides a difference signal indicative of the difference on a line 130. The difference signal is input to resolver folder over logic 132. FIG. 7 is a block diagram illustration of the resolver folder over logic. This logic accounts for the resolver data captured near and through the resolver points. Velocity is counted as long as the clock signal is active. The fold over logic 132 provides an output signal to a counter 134 (e.g., a ten bit counter) that provides a signed PWM output (e.g., 0 to 5 VDC) on the line 40 indicative of velocity. For example, zero velocity is

represented by 50% duty cycle, while full-scale negative velocity is represented by 0% duty cycle and full scale positive velocity is represented by 100% duty cycle. The counter 134 preferably also includes overflow protection to ensure that if velocity exceeds a certain threshold (e.g., ±5,493 RPM), then the 0% or 100% duty cycle is provided depending of course of the polarity of the velocity. Down stream external bipolar filtering and offset provided by filter 150 (FIG. 1) provides the signed positive and negative velocity feedback voltage scaling.

Although the present invention has been discussed in the context of working with a four pole motor and a two pole resolver, one of ordinary skill will of course appreciate the present invention is certainly not limited to such systems.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: